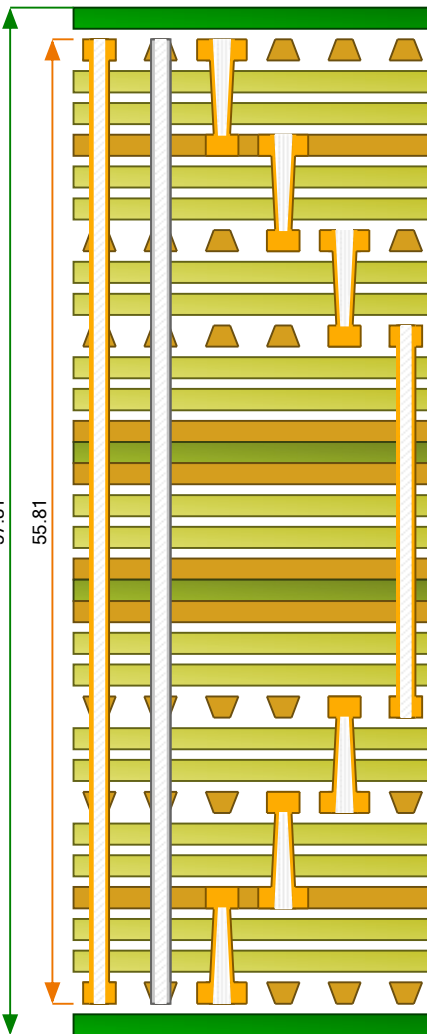



Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID	
1		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500		
		Copper Foil 12 microns-HTE	1.850		100.000		1, 2	
		Iteq IT180A Prepreg 106 RC71.5-NEW	1.893	3.786		3.790		
		Iteq IT180A Prepreg 106 RC71.5-NEW	1.893	-		3.790		
2		Copper Foil 9 microns-HTE	1.379		80.000			
		Iteq IT180A Prepreg 106 RC71.5-NEW	1.755	3.510		3.790		
		Iteq IT180A Prepreg 106 RC71.5-NEW	1.755	-		3.790		
		3	Copper Foil 9 microns-HTE	1.379		60.000		3, 4, 5
Iteq IT180A Prepreg 106 RC71.5-NEW			1.755	3.510		3.790		
Iteq IT180A Prepreg 106 RC71.5-NEW			1.755	-		3.790		
4			Copper Foil 9 microns-HTE	1.379		60.000		6, 7
		Iteq IT180A Prepreg 106 RC71.5-NEW	1.905	3.810		3.790		
	Iteq IT180A Prepreg 106 RC71.5-NEW	1.905	-		3.790			
	5	Copper Foil 9 microns-HTE	1.260		80.000			
Iteq IT180A 3 mil core 1/1		3.000	3.000		3.930			
Iteq IT180A Prepreg 106 RC71.5-NEW		1.779	3.558		3.790			
Iteq IT180A Prepreg 106 RC71.5-NEW		1.779	-		3.790			
7	Copper Foil 9 microns-HTE	1.260		80.000				
	Iteq IT180A 3 mil core 1/1	3.000	3.000		3.930			
	Copper Foil 9 microns-HTE	1.260		80.000				
	8	Iteq IT180A Prepreg 106 RC71.5-NEW	1.905	3.810		3.790		
Iteq IT180A Prepreg 106 RC71.5-NEW		1.905	-		3.790			
9		Copper Foil 9 microns-HTE	1.379		60.000		8, 9	
		Iteq IT180A Prepreg 106 RC71.5-NEW	1.755	3.510		3.790		
	Iteq IT180A Prepreg 106 RC71.5-NEW	1.755	-		3.790			
	10	Copper Foil 9 microns-HTE	1.379		60.000		10, 11, 12	
Iteq IT180A Prepreg 106 RC71.5-NEW		1.755	3.510		3.790			
Iteq IT180A Prepreg 106 RC71.5-NEW		1.755	-		3.790			
11		Copper Foil 9 microns-HTE	1.379		80.000			
	Iteq IT180A Prepreg 106 RC71.5-NEW	1.893	3.786		3.790			
	Iteq IT180A Prepreg 106 RC71.5-NEW	1.893	-		3.790			
	12	Copper Foil 12 microns-HTE	1.850		100.000		13, 14	
Taiyo PSR 4000 HFX DI-GREEN		1.000			3.500			

Copper Thickness = 17.014 | Dielectric Thickness = 38.792 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 55.806 | Stack Up Thickness with Soldermask = 57.806

StackName: Master	Version:	Revision:	Modification:	Date of Revision:	Editor	Pag	
Date: 02-01-2025	Associated Documents:						
Author: -							
Department: Engg-CAM							
Site: www.hiqelectronics.com							



Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)	
1	1	Edge Coupled Coated Microstrip 1B	2	0	4.000	5.400	0.000	99.810	100.000	10.000	
2	1	Coated Microstrip 1B	2	0	6.400	0.000	0.000	49.990	50.000	10.000	
3	3	Edge Coupled Offset Stripline 1B1A	2	5	3.500	8.000	0.000	100.000	100.000	10.000	
4	3	Offset Stripline 1B1A	2	5	4.000	0.000	0.000	50.400	50.000	10.000	
5	3	Edge Coupled Offset Stripline 1B1A	2	5	3.800	5.200	0.000	90.140	90.000	10.000	
6	4	Edge Coupled Offset Stripline 1B1A	2	5	3.500	7.500	0.000	100.080	100.000	10.000	
7	4	Offset Stripline 1B1A	2	5	4.200	0.000	0.000	50.010	50.000	10.000	
8	9	Offset Stripline 1B1A	8	11	4.200	0.000	0.000	50.010	50.000	10.000	
9	9	Edge Coupled Offset Stripline 1B1A	8	11	3.500	7.500	0.000	100.080	100.000	10.000	
10	10	Edge Coupled Offset Stripline 1B1A	8	11	3.800	5.200	0.000	90.140	90.000	10.000	
11	10	Offset Stripline 1B1A	8	11	4.000	0.000	0.000	50.400	50.000	10.000	
12	10	Edge Coupled Offset Stripline 1B1A	8	11	3.500	8.000	0.000	100.000	100.000	10.000	
13	12	Coated Microstrip 1B	11	0	6.400	0.000	0.000	49.990	50.000	10.000	
14	12	Edge Coupled Coated Microstrip 1B	11	0	4.000	5.400	0.000	99.810	100.000	10.000	

Notes

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